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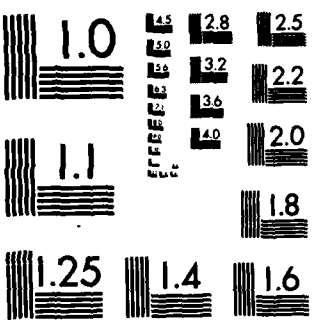

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Final Technical Report

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Test Procedures and Design Methods for Reliable Large Scale Integrated Circuits and Systems

Submitted by

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The following four major problem areas were investigated in the course of the research supported: (1) procedures to detect faults in random access memories; (2) analysis and design of fault-tolerant computing networks; (3) design of testable microprocessors and iterative logic arrays; and (4) design and analysis of fault-tolerant connection networks.

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1. Summary of Results Obtained:

The following four major problem areas were investigated in the course of the research supported:

(i) procedures to detect faults in random access memories

(ii) analysis and design of fault-tolerant computing networks

(iii) design of testable microprocessors and iterative logic arrays and (iv) design and analysis of fault-tolerant connection networks.

The results derived have all been presented in major technical publications and conference proceedings. Summaries of the results obtained are given below:

(i) Random Access Memory Faults: Optimal procedures to detect functional and a class of pattern sensitive faults have been derived [1-4, a]*. The procedures allow the detection of most probable faults in static and dynamic random access memories

(ii) Computing Networks: A model for distributed fault-diagnosis and fault tolerance was proposed [8]. Various methods to analyze and design fault-tolerant distributed computing networks and methods for recovery in the presence of faults were studied [8, 10, 12, 13, 15, 18, 19, 21, 22, 24].

(iii) Testable Microprocessors: A method to design testable microprocessors, which involved the design of address bus as a bidirectional bus proposed and analyzed [17, 25]. Methods to derive testable iterative logic arrays were studied [5, 16]. The results in this latter area are applicable to the design of bit sliced machines.

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*References are given in the publications section.

(iv) Connection networks: Connection networks are used for high bandwidth connections between processors or processors and memories. Methods to analyze and design fault-tolerant connection networks were investigated [7, 55].

(v) Problems in fault diagnosis: Several problems in fault diagnosis in general logic networks were investigated [6, 20, 23]. The most important result was the observation that transistor stuck-open faults in CMOS logic networks pose difficulties in designing tests to detect them due to circuit delays [23]. Methods to design CMOS Logic circuits that are testable in the presence of arbitrary circuit delays were proposed [23].

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II. List of Publications:

Papers

1. Suk, D.S. and Reddy, S.M., "A Fault Detecting Test for Semiconductor Random Access Memories," 16th Annual Allerton Conference on Computing and System Theory, October 1978.

2. Suk, D.S. and Reddy, S.M., "A March Test for Functional Faults in Semiconductor Random Access Memories," IEEE Trans. Comp., pp. 982-985, December 1981.

3. Suk, D.S. and Reddy, S.M., "An Algorithm to Detect a Class of Pattern Sensitive Faults in Semiconductor Random Access Memories," Proceedings of the International Symposium on Fault-Tolerant Computing, pp. 219-226, June 1979.

4. Reddy, S.M., "A Procedure to Detect Stuck-at-Faults in Dynamic Random Access Memories," Proceedings of the 1979 Conference on Information Sciences and Systems, pp. 310-313, March 1979.

5. Parthasarathy, R. and Reddy, S.M., "On Fault Diagnosis of Iterative Logic Arrays," Proceedings of Seventeenth Annual Allerton Conference on Communication, Control and Computing, October 1979.

6. Reddy, S.M., "Fault Diagnosis by Compressed Test Data," 17th Annual Allerton Conference on Computing, Controls and Communication, October 1979.

7. Sowrirajan, S. and Reddy, S.M., "A Design for Fault-Tolerant Full Connection Networks," Proceedings of the 1980 Conference on Information Sciences and Systems, pp. 536-540, March 1980.

8. Kuhl, J.G. and Reddy, S.M., "Distributed Fault-Tolerance for Large Multiprocessor Systems," Proceedings of the 7th Annual Computer Architecture Conference, pp. 23-30, May 1980.

9. Suk, D.S. and Reddy, S.M., "Test Procedures for a Class of Pattern-Sensitive Fault in Semiconductor Random Access Memories," IEEE Transactions on Computers, pp. 419-429, June 1980.

10. Kuhl, J.G. and Reddy, S.M., "Some Extensions to the Theory of System Level Fault Diagnosis," Digest of Papers of the 10th International Symposium on Fault-Tolerant Computing, pp. 291-296, October 1980.

11. Saluja, K.K. and Reddy, S.M., "A Class of Undirected Graphs, Proc. of the 15th Annual Conference on Information Sciences and Systems, pp. 388-393, March 1981.

12. Kuhl, J.G. and Reddy, S.M., "Fault Diagnosis in Fully Distributed Computing Systems," Proc. 11th International Symp. on Fault-Tolerant Computing, June 1981.

II. Papers (continued)

13. Pradhan, D.K. and Reddy, S.M., "A Fault-Tolerant Communication Architecture for Distributed Systems," The 11th Annual International Symposium on Fault-Tolerant Computing, pp. 214-219, June 1981.

14. Sowrirajan, S. and Reddy, S.M., "Fault Diagnosis and Fault-Tolerance in Concentrators," Proceedings of the International Conference on Parallel Processing, August 1981.

15. Kuhl, J.G. and Reddy, S.M., "Some Properties of the Binary N-Cube as a Network Interconnection Structure", Procedings of the Nineteenth Annual Allerton Conference on Communication, Control and Systems, September 1981.

16. Parthasarathy, R. and Reddy, S.M., "A Testable Design of Iterative Logic Arrays," IEEE Transactions on Computers, pp. 833-842, November 1981.

17. Parthasarathy, R., Reddy, S.M. and Kuhl, J.G., "A Testable Design of General Purpose Microprocessors," Proceedings of 12th International Symposium on Fault-Tolerant Computing, June 1982.

18. Pradhan, D.K. and Reddy, S.M., "A Fault-Tolerant Communication Architecture for Distributed Systems," IEEE Transactions on Computers, pp. 863-870, September 1982.

19. Reddy, S.M., Kuhl, J.G., Hosseini, S.H. and Lee, H., "On Digraphs with Minimum Diameter and Maximum Connectivity," in Proc. of the 20th Annual Allerton Conference on Circuits and Systems, October 1982.

20. Reddy, S.M., Reddy, M.K. and Kuhl, J.G., "Testable Design for Stuck-at-Open Faults in CMOS Logic Circuits," Sixth Annual Workshop on Design for Testability, Vail, Colorado, April 13,14, 1983.

21. Hosseini, S.H., Kuhl, J.G. and Reddy, S.M., "An Integrated Approach to Error Recovery in Distributed Computing Systems," Proc. of 12th International Symposium on Fault-Tolerant Computing, pp. 56-63, June 1983.

22. Reddy, S.M., Raghavan, P. and Kuhl, J.G., "A Class of Graphs for Processor Interconnection," Proceedings of the 1983 International Conference on Parallel Processing, pp. 154-157, August 1983.

23. Reddy, S.M., Reddy, M.K. and Kuhl, J.G., "On Testable Design for CMOS Logic Circuits," Proceedings of 1983 International Test Conference, pp. 435-445, October 1983.

24. Hosseini, S.H., Kuhl, J.G. and Reddy, S.M., "A Diagnosis Algorithm for Distributed Computing Systems with Dynamic Failure and Repair," to be published in IEEETC.

25. S. Nanda and S.M. Reddy, "Design of Easily Testable Microprocessors - Case Study", Proceedings of 1982 International Test Conference, pp. 480-483, November 1982.

II. List of Publications (continued):

Theses

1. D.S. Suk, "Functional and Pattern Sensitive Fault Testing Algorithms for the Semiconductor Random Access Memories", Ph.D. Thesis Electrical Engineering, The University of Iowa, Iowa City, Iowa, July 1978.

2. J.G. Kuhl, "Fault Diagnosis in Computing Networks", Ph.D. Thesis, University of Iowa, Iowa City, Iowa, July 1980.

3. S. Sowrirajan, "Fault Diagnosis and Fault-Tolerance in Connection Networks", Ph.D. Thesis, Electrical and Computer Engineering. University of Iowa, July 1981.

4. R. Parthasaratny, "Easily Testable LSI Digital Circuits", Ph.D. Thesis, Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, December 1981.

5. S. Nanda, "A Gate Level Logic Simulator for Sequential Machines", M.S. Thesis, Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, May 1982.

6. S.H. Hosseini, "Fault-Tolerance in Distributed Computing Systems and Data Bases", Ph.D. Thesis, Electrical and Computer Engineering, University of Iowa, Iowa City, Iowa, August 1982.

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